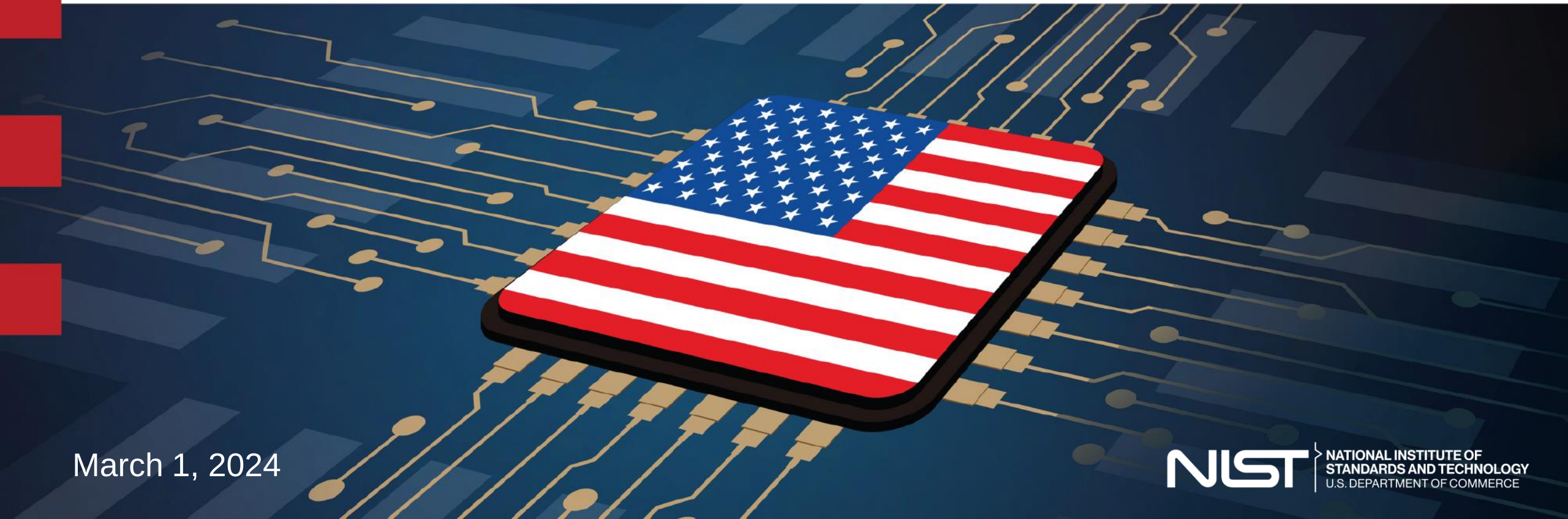
CHIPS for America Substrates and Substrate Materials Program



March 1, 2024

NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

Today's Speakers

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NAPMP

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Materials and Substrates

Disclaimer

- Statements and responses to questions about advanced microelectronics research and development programs in this webinar:
  - Are informational, pre-decisional, and preliminary in nature.
  - Do not constitute a commitment and are not binding on NIST or the Department of Commerce.
  - Are subject in their entirety to any final action by NIST or the Department of Commerce.
- Nothing in this presentation is intended to contradict or supersede the requirements published in any future policy documents or Notices of Funding Opportunity.

Webinar Expectations

Agenda

- CHIPS R&D Program
- Substrates and Substrate Materials Program
- Materials and Substrates Proposer's Day

By the end, attendees should better understand

- Outcomes of the Materials and Substrates Program
- Key Dates in the Materials and Substrates Funding Opportunity
- Materials and Substrates Proposer's Day Details

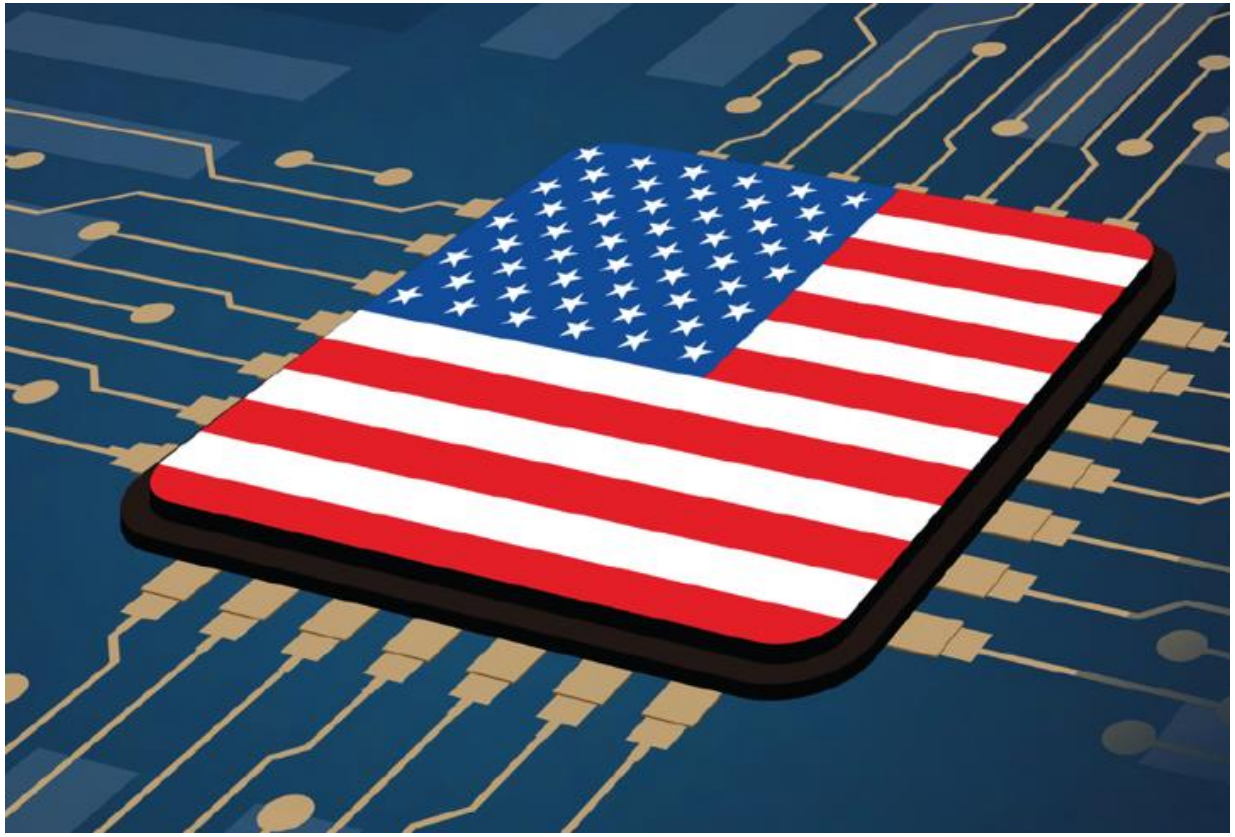
CHIPS R&D

Vision

A vibrant and self-sustaining U.S. domestic semiconductor ecosystem that revitalizes American manufacturing, grows a skilled and diverse workforce, and leads the world in semiconductor research and innovation.

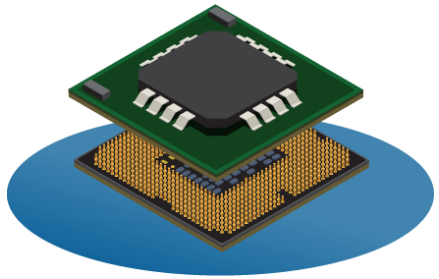
Mission

Accelerate the development and commercial deployment of foundational semiconductor technologies by establishing, connecting, and providing access to domestic research efforts, tools, resources, workers, and facilities.



CHIPS R&D Programs

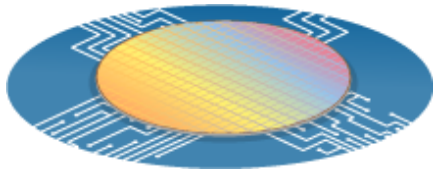
Metrology Program



National Semiconductor Technology Center

Natcast

Natcast is an independent nonprofit organization and operator of the NSTC consortium



National Advanced Packaging Manufacturing Program

Manufacturing USA

CHIPS Manufacturing USA

Workforce Initiatives

Establishing Advanced Packaging in the U.S.

Packaging Roadmaps

- NIST-sponsored roadmaps: MRHIEP, MAESTRO and MAPT
- Other roadmaps: HIR and IRDS

Technology Investment Areas

- All aspects of technologies required to develop a leading-edge on-shore advanced packaging manufacturing capability

The National Advanced Packaging Piloting Facility (NAPPF)

- Key to facilitating high-volume manufacturing
- Piloting and prototyping functions

The Chiplet and Design Ecosystem

- Chiplet discovery, disaggregation and reaggregation methodologies, protocols, standards, fabrication and warehousing design for test, repair and reliability, and holistic design tools and methodologies

Design in the U.S., build in the U.S., and sell worldwide

- Successful development efforts will be transitioned and validated for scaled transition to U.S. manufacturing

NAPMP Priority Research Investment Areas

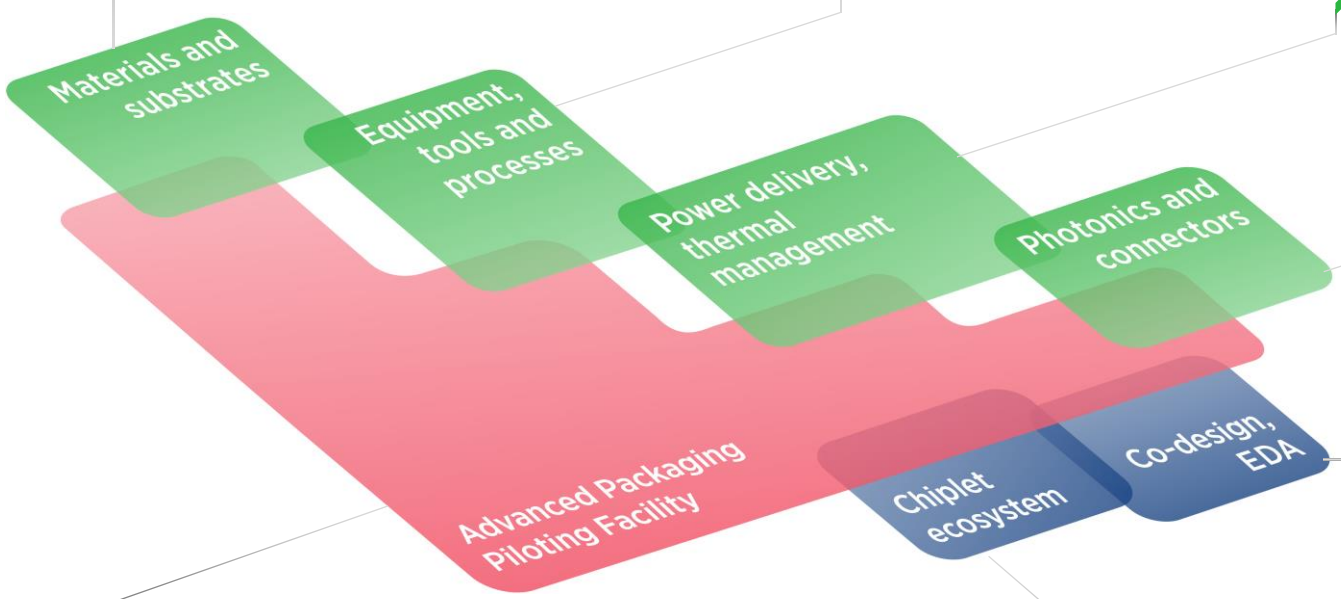
Materials and substrates are the platform for heterogeneous integration of dielets

Equipment, tools, and processes are needed to pattern substrates and assemble dielets and passivate assemblies

Thermal management and efficient power delivery are critical needs

Photonics and connectors allow the assembly to interact with the outside world

Automated design for test, repair, security, and reliability; substrate and process dependent



The NAPPF provides a test bed for integration of the different investment areas and also functions as a piloting and prototyping facility

The chiplet ecosystem is crucial for any implementation of advanced packaging

NAPPF: National Advanced Packaging Piloting Facility

Substrates and Substrate Materials Program

Substrates and Substrate Materials Program

Vision & Mission

- The Program vision is to drive **U.S. leadership** in advanced substrates manufacturing for advanced packaging in the United States
- The program mission is to develop **critical and relevant innovations** for advanced substrates to enable **cutting edge advanced packaging applications** and **scale up** substrate innovations **into U.S. manufacturing**

Objectives

1. Accelerate domestic R&D and innovation in advanced packaging materials and substrates;
2. Translate domestic materials and substrate innovation into U.S. manufacturing, such that these technologies are available to U.S. manufacturers and customers, including to significantly benefit U.S. economic and national security;
3. Support the establishment of a robust, sustainable, domestic capacity for advanced packaging materials and substrate R&D, prototyping, commercialization, and manufacturing; and
4. Promote a skilled and diverse pipeline of workers for a sustainable domestic substrate manufacturing sector.

Approach

1

Scale down: shrinking features on a package:

- ✓ Making the features on the package approach those at the top level on a monolithic CMOS chip
- ✓ Reducing the distance between dies that are assembled on a multi-chip package to approach the distance between IP blocks on a monolithic chip

2

Scale out: increasing the areal density of chips on a package

- ✓ Accommodate a larger number of closely packed heterogeneous die
- ✓ Address the power delivery, thermal dissipation and external connection challenges
- ✓ Develop standards and protocols to accommodate a large and diverse set of chips (chiplets)

3

R&D that leads to sustainable manufacturing at appropriate volume

- ✓ Translate domestic materials and substrate innovation into U.S. manufacturing
- ✓ Promote a skilled and diverse pipeline of workers for a sustainable domestic substrate manufacturing sector

Program Scope

3 Technical Areas

- Organic substrates, including fan-out.
- Glass-based substrates
- Semiconductor-based substrates

Flexible and substrates for biomedical applications

Applicants can propose to one or more technical areas

Activities

TECHNICAL

- Basic and applied R&D
- Substrate development
- Demonstration device development

NON-TECHNICAL

- Commercial viability
- Workforce development
- Domestic Production

Awards

- $300 Million total over 5 years
- Individual awards up to $100 Million

Co-investment not required. It is encouraged.

Substrates and Substrate Materials

What is within program scope?

- Substrate wiring
- Via pitches
- Through substrate vias
- Number of levels on both sides of the substrate
- One or more passive or active components embedded in the substrate for enhanced functionality

What is NOT within program scope?

- Traditional boards
- Interposers
- Small area substrates

Materials and Substrates Funding Opportunity

- Follow QR code for full text of funding opportunity
- Sections to provide as much detail for applicants:
  - **Funding opportunity description** (*project-level activities, structure, and technical areas and targets*)
  - **Project-level Non-Technical Targets** (*workforce, commercial viability, domestic production*)
  - **Demonstration Devices**
  - **Broader Impacts** (*future Investments, support for other R&D, inclusive opportunities, environmental, and community impact*)
  - **Research Security**, **Eligibility**, and **Application Process**
- Encourage those interested to familiarize themselves and direct questions to research@chips.gov with "2024-NIST-CHIPS-NAPMP-01 Questions“ in subject.

CHIPS for America QR Code: **CHIPS NAPMP Materials and Substrates NOFO** (full text)

Materials and Substrates NOFO: key dates

February 28, 2024

Materials and Substrates Funding Opportunity (Released)

For R&D activities that will **establish and accelerate domestic capacity for advanced packaging substrates and substrate materials**

March 12, 2024

Materials and Substrates Proposer's Day

Share detailed information on Materials and Substrates NOFO, in a collaborative atmosphere

Due: April 12, 2024

Concept Papers Review

Mandatory concept papers submitted by teams

Teams invited to submit full application

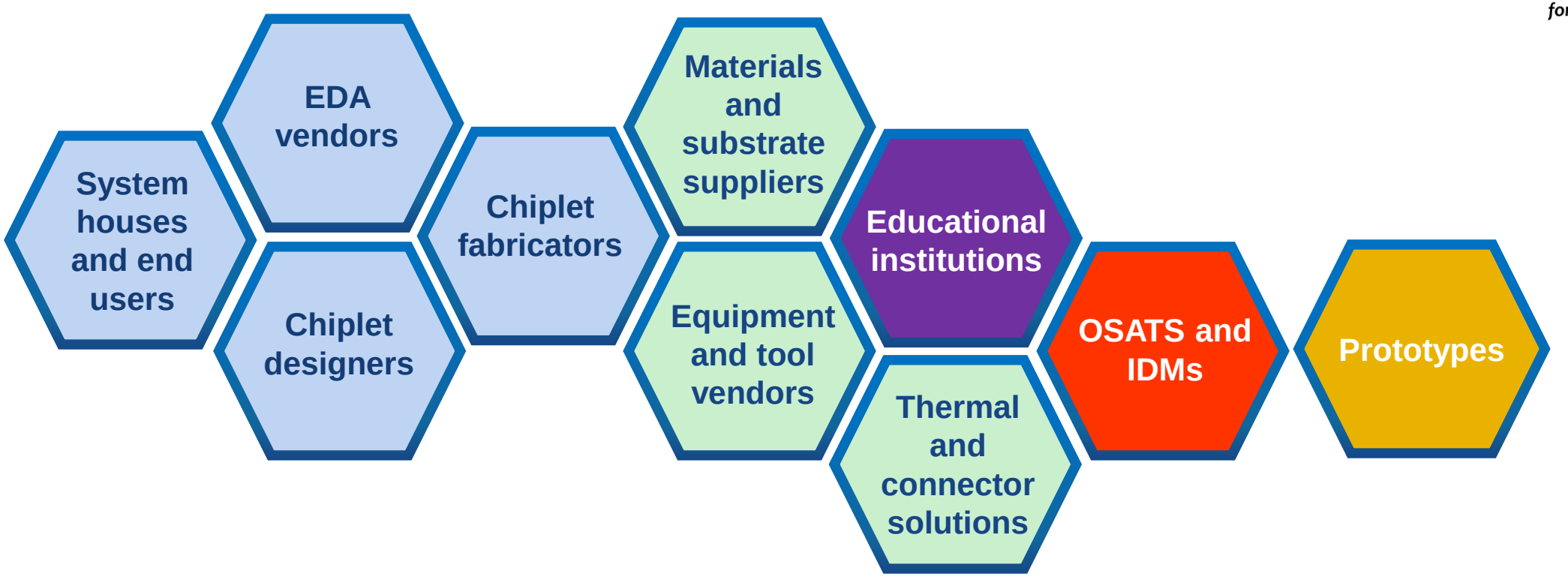
July 3, 2024

Full Application Due

The full application from applicants due

CHIPS for America QR Code: **CHIPS NAPMP Materials and Substrates NOFO** (full text)

Collaboration is Critical for Success



We encourage you to begin identifying your individual contributions to the ecosystem as well as partners who can help accomplish the vision and goals of the NAPMP.

Next Steps

Materials and Substrates Proposer's Day

- One day event on March 12, 2024
- Hilton Rockville Executive Meeting Center in Rockville, MD
- Hybrid Meeting, In-person attendance is strongly encouraged.
  - Plenary session describing Materials and Substrates Notice of Funding Opportunity requirements and submission process in detail
  - Breakout sessions to facilitate networking among attendees. Virtual attendees will have a breakout session.
- **Learn more and register at CHIPS.gov under Events**
- Registration will close March 5, 2024. Please Register!

CHIPS for America QR Code:
CHIPS NAPMP Proposer's Day
(event webpage)

Frequently Asked Questions

Frequently Asked Questions

Can applicants receive money from both the $39 billion for incentives and the $11 billion for R&D?

Yes, applicants can receive funding from both programs if the applicant can show the Department how its proposed projects / uses of funding would advance the individual objectives of each program.

Frequently Asked Questions

Are there non-technical targets applicants should consider?

Yes, the Education and Workforce Development and Commercial Viability and Domestic Production Targets are described in section 1.6.

Frequently Asked Questions

What successful outcomes do you expect to come out from the award recipient's research?

This funding opportunity seeks applications for activities that will achieve the following objectives:

- Accelerate domestic R&D and innovation in advanced packaging materials and substrates;
- Transition domestic materials and substrate innovation into U.S. manufacturing, such that these technologies are available to U.S. manufacturers and customers, including to significantly benefit U.S. economic and national security; and
- Promote a skilled and diverse pipeline of workers for a sustainable domestic substrate manufacturing sector.

Frequently Asked Questions

Is there an opportunity to meet potential team members?

CHIPS R&D encourages collaborative proposals under this NOFO. Though not required, CHIPS R&D expects that applicants assembling teams may be best suited to collectively provide the full range of expertise and capabilities needed to achieve the program objectives, including the proposed project-level targets.

The Materials and Substrates Proposer's Day on March 12, 2024 will provide opportunities for networking.

Thank You

Direct additional questions to **research@chips.gov** with 2024-NIST-CHIPS-NAPMP-01 in subject.